CLAIMS

1. A method for programming a charge storage memory cell having a source and a drain in a substrate, a charge storage element, and a control gate, comprising:

applying a gate voltage to the control gate relative to a reference voltage, a source voltage to the source relative to the reference voltage, and a drain voltage to the drain relative to the reference voltage, in an operation to induce charge transfer to the charge storage element and establish a threshold voltage for the memory cell;

increasing the drain voltage during the operation; and

increasing the source voltage while increasing the drain voltage during the operation.

2. The method of claim 1, wherein the operation is self-converging during a portion of the program operation in which the voltage threshold converges on an ending threshold.

3. The method of claim 1, including holding the gate voltage substantially constant during a portion of the program operation in which the voltage threshold converges on an ending threshold.

4. The method of claim 1, including holding the gate voltage substantially constant during the program operation.

5. The method of claim 1, wherein the memory cell has a drain-to-source voltage between the source and the drain, including holding the gate voltage substantially constant during the program operation, and holding the drain-to-source voltage substantially constant during the program operation.

6. The method of claim 1, wherein the applying includes applying a sequence of source voltage pulses to the source, and said increasing the source voltage comprises increasing the source voltage pulse heights in successive pulses in the sequence, and

applying a sequence of drain voltage pulses to the drain of the memory cell during the operation and said increasing the drain voltage comprises increasing the drain voltage pulse heights in successive pulses in the sequence.

7. The method of claim 1, wherein the applying includes applying a sequence of source voltage pulses to the source, and said increasing the source voltage comprises increasing the source voltage pulse heights in successive pulses in the sequence, and applying a sequence of drain voltage pulses to the drain of the memory cell during the operation and said increasing the drain voltage comprises increasing the drain voltage pulse heights in successive pulses in the sequence; and including

applying verify pulses between successive pulses in the sequence.

8. The method of claim 1, wherein the applying includes applying a ramped source voltage to the source and a ramped drain voltage to the drain of the memory cell during the operation.

9. The method of claim 1, including holding the gate voltage substantially constant during the operation, and wherein said increasing the source and drain voltages comprises stepping the source and drain voltages by substantially equal steps during the operation.

10. The method of claim 1, including coupling the substrate to the reference voltage during the operation.

11. The method of claim 1, wherein said charge storage element in the memory cell comprises a non-conductive charge trap.

12. The method of claim 1, wherein said charge storage element in the memory cell comprises a conductive floating gate.

13. The method of claim 1, wherein said memory cell comprises an NROM cell.

14. The method of claim 1, wherein said memory cell comprises a flash memory cell.

15. The method of claim 1, wherein the memory cell is adapted to store a plurality of bits, and including setting the gate voltage to one of a predetermined set of gate voltages during the operation to establish one of a corresponding set of threshold voltages in the memory cell.

16. The method of claim 1, including applying another program operation to induce charge trapping on another side of the memory cell, including

applying a gate voltage to the control gate of the selected memory cell relative to a reference voltage, a source voltage to the second terminal of the selected memory cell relative to the reference voltage, and a drain voltage to the first terminal of the selected memory cell, relative to the reference voltage;

increasing the drain voltage during the operation; and

increasing the source voltage while increasing the drain voltage during the operation.

17. A method for programming a multi-level charge storage memory cell having a first terminal and a second terminal acting as sources and drains in a substrate, a charge storage element, and a control gate, comprising:

determining a data value from one of more than two data values to be stored in the memory cell;

applying a gate voltage to the control gate relative to a reference voltage, a source voltage to the first terminal relative to the reference voltage, and a drain voltage to the second terminal relative to the reference voltage, in a program operation to induce charge transfer to the charge storage element to establish a threshold voltage for the memory cell;

holding the gate voltage substantially constant at one of a predetermined set of gate voltages in response to the determined data value during a portion of the program operation in which the voltage threshold converges on a target threshold corresponding with the determined data value;

increasing the drain voltage during the operation; and

increasing the source voltage while increasing the drain voltage during the operation.

18. The method of claim 17, wherein the operation is self-converging during a portion of the program operation in which the voltage threshold converges on an ending threshold.

19. The method of claim 17, wherein the memory cell has a drain-to-source voltage between the first and second terminals, including holding the drain-to-source voltage substantially constant during the program operation.

20. The method of claim 17, wherein the applying includes applying a sequence of source voltage pulses to the first terminal, and said increasing the source voltage comprises increasing the source voltage pulse heights in successive pulses in the sequence, and applying a sequence of drain voltage pulses to the second terminal of the memory cell during the operation and said increasing the drain voltage comprises increasing the drain voltage pulse heights in successive pulses in the sequence.

21. The method of claim 17, wherein the applying includes applying a sequence of source voltage pulses to the first terminal, and said increasing the source voltage comprises increasing the source voltage pulse heights in successive pulses in the sequence, and applying a sequence of drain voltage pulses to the second terminal of the memory cell during the operation and said increasing the drain voltage comprises increasing the drain voltage pulse heights in successive pulses in the sequence; and including

applying verify pulses between successive pulses in the sequence.

22. The method of claim 17, wherein the applying includes applying a ramped source voltage to the first terminal and a ramped drain voltage to the second terminal of the memory cell during the operation.

23. The method of claim 17, wherein said increasing the source and drain voltages comprises stepping the source and drain voltages by equal steps during the operation.

24. The method of claim 17, including coupling the substrate to the reference voltage during the operation.

25. The method of claim 17, wherein said charge storage element in the memory cell comprises a non-conductive charge trap.

26. The method of claim 17, wherein said charge storage element in the memory cell comprises a conductive floating gate.

27. The method of claim 17, wherein said memory cell comprises an NROM cell.

28. The method of claim 17, wherein said memory cell comprises a flash memory cell.

29. The method of claim 17, including applying another program operation to induce charge trapping on another side of the memory cell, including

applying a gate voltage to the control gate of the selected memory cell relative to a reference voltage, a source voltage to the second terminal of the selected memory cell relative to the reference voltage, and a drain voltage to the first terminal of the selected memory cell, relative to the reference voltage;

increasing the drain voltage during the operation; and

increasing the source voltage while increasing the drain voltage during the operation.

30. An integrated circuit, comprising:

a memory array including decoding circuitry to select memory cells for programming, the memory cells having first and second terminals in a substrate acting as

sources and drains, a charge storage element, and a control gate, wherein said charge storage element in the memory cell comprises a non-conductive charge trap;

a voltage supply circuit coupled to the memory array adapted to apply a gate voltage, a source voltage and a drain voltage to the control gate, first terminal and second terminal, respectively, of memory cells in the array; and

a program controller coupled to the decoding circuitry and to the voltage supply circuit, the program controller adapted to execute a self-converging program operation for a selected memory cell to induce charge transfer to the charge storage element and establish a threshold voltage for the selected memory cell.

31. The integrated circuit of claim 30, wherein said memory cell comprises an NROM cell.

32. The integrated circuit of claim 30, wherein the memory cell is adapted to store a plurality of bits, and the program operation establishes one of a set of threshold voltages corresponding with the plurality of bits in the memory cell.

33. An integrated circuit, comprising:

a memory array including decoding circuitry to select memory cells for programming, the memory cells having first and second terminals in a substrate acting as sources and drains, a charge storage element, and a control gate;

a voltage supply circuit coupled to the memory array adapted to apply a gate voltage, a source voltage and a drain voltage to the control gate, first terminal and second terminal respectively, of memory cells in the array; and

a program controller coupled to the decoding circuitry and to the voltage supply circuit, the program controller adapted to execute a program operation for a selected memory cell to induce charge transfer to the charge storage element and establish a threshold voltage for the selected memory cell, the program operation including

applying a gate voltage to the control gate of the selected memory cell relative to a reference voltage, a source voltage to the first terminal of the selected memory cell

relative to the reference voltage, and a drain voltage to the second terminal of the selected memory cell, relative to the reference voltage;

increasing the drain voltage during the operation; and

increasing the source voltage while increasing the drain voltage during the operation.

34. The integrated circuit of claim 33, wherein the operation is self-converging during a portion of the program operation in which the voltage threshold converges on an ending threshold.

35. The integrated circuit of claim 33, including holding the gate voltage substantially constant during a portion of the program operation in which the voltage threshold converges on an ending threshold.

36. The integrated circuit of claim 33, including holding the gate voltage substantially constant during the program operation.

37. The integrated circuit of claim 33, wherein the memory cell has a drain-to-source voltage between the first and second terminals, including holding the gate voltage substantially constant during the program operation, and holding the drain-to-source voltage substantially constant during the program operation.

38. The integrated circuit of claim 33, wherein the applying includes applying a sequence of source voltage pulses to the first terminal, and said increasing the source voltage comprises increasing the source voltage pulse heights in successive pulses in the sequence, and applying a sequence of drain voltage pulses to the second terminal of the memory cell during the operation and said increasing the drain voltage comprises increasing the drain voltage pulse heights in successive pulses in the sequence.

39. The integrated circuit of claim 33, wherein the applying includes applying a sequence of source voltage pulses to the first terminal, and said increasing the source

voltage comprises increasing the source voltage pulse heights in successive pulses in the sequence, and applying a sequence of drain voltage pulses to the second terminal of the memory cell during the operation and said increasing the drain voltage comprises increasing the drain voltage pulse heights in successive pulses in the sequence; and including

applying verify pulses between successive pulses in the sequence.

40. The integrated circuit of claim 33, wherein the applying includes applying a ramped source voltage to the first terminal and a ramped drain voltage to the second terminal of the memory cell during the operation.

41. The integrated circuit of claim 33, including holding the gate voltage substantially constant during the operation, and wherein said increasing the source and drain voltages comprises stepping the source and drain voltages by substantially equal steps during the operation.

42. The integrated circuit of claim 33, wherein the substrate is coupled to the reference voltage during the operation.

43. The integrated circuit of claim 33, wherein said charge storage element in the memory cell comprises a non-conductive charge trap.

44. The integrated circuit of claim 33, wherein said charge storage element in the memory cell comprises a conductive floating gate.

45. The integrated circuit of claim 33, wherein said memory cell comprises an NROM cell.

46. The integrated circuit of claim 33, wherein said memory cell comprises a flash memory cell.

47. The integrated circuit of claim 33, wherein the memory cell is adapted to store a plurality of bits, and the program operation includes setting the gate voltage to one of a predetermined set of gate voltages during the operation to establish one of a corresponding set of threshold voltages in the memory cell.

48. The integrated circuit of claim 33, wherein the program controller is adapted to apply another program operation to induce charge trapping on another side of the memory cell, including

applying a gate voltage to the control gate of the selected memory cell relative to a reference voltage, a source voltage to the second terminal of the selected memory cell relative to the reference voltage, and a drain voltage to the first terminal of the selected memory cell, relative to the reference voltage;

increasing the drain voltage during the operation; and

increasing the source voltage while increasing the drain voltage during the operation.

49. An integrated circuit, comprising:

a memory array including decoding circuitry to select memory cells for programming, the memory cells having first and second terminals in a substrate acting as sources and drains, a charge storage element, and a control gate;

a voltage supply circuit coupled to the memory array adapted to apply a gate voltage, a source voltage and a drain voltage to the control gate, first terminal and second terminal respectively, of memory cells in the array; and

a program controller coupled to the decoding circuitry and to the voltage supply circuit, the program controller adapted to execute a program operation for a selected memory cell to induce charge transfer to the charge storage element on first and second sides of the memory cell, and establish threshold voltages on the first and second sides of the selected memory cell, the program operation including storing more than one bit of information in each of the first and second sides of the memory cell.